

IN THE CLAIMS

Please substitute claims 1, 2, 3 and 18 as attached hereto for claims 1, 2, 3 and 18 of record. A copy of the claims showing the amendments thereto, along with a copy of all of the pending claims in the application, is attached.

## CLAIMS:

**1. (Currently Amended)** A signal processing circuit outputting an output signal corresponding to a pulse width of an input pulse signal, the circuit comprising:

a first and second charging circuit,

means for applying a gradually changing charge on said first charging circuit when said input pulse signal is of positive polarity and for applying a gradually changing charge on said second charging circuit when said input pulse signal is of negative polarity for a predetermined period of time including at least one pulse which permits a noise component to be superimposed thereon;

means for sampling and holding the charge accumulated in each of the first and second charging circuits so as to generate said output signal;

~~means for accumulating the pulse widths of said input pulse signal for a predetermined period of time, with each of the pulses having one of polarities having one of positive and negative polarities; and~~

~~outputting means for outputting the output signal corresponding to said accumulated pulse widths~~ corresponding to the pulse width of each input pulse based on the charge accumulated in one of the first and second charging circuits.

**2. (Currently Amended)** The signal processing circuit as claimed in claim 1, wherein said ~~integrating means comprises a charging circuit~~ means for sampling and holding comprises a sample hold circuit for sampling and holding the ~~charging circuit storing a charged voltage according to one~~ either of polarities of said input pulse signal; and

~~— a sample hold circuit sampling and holding the charged voltage stored according to one of said polarities, during a period of supply of said input pulse signal having the other of said polarities in which no chattering is generated in the input pulse signal during the period.~~

**3. (Currently Amended)** The signal processing circuit as claimed in claim 2, wherein said first and second charging circuit includes:

~~— a first charge circuit charged with a first constant current during a period of said input pulse signal having a positive polarity; and~~

~~— a second charge circuit charged with a second constant current during a period of said input pulse signal having a negative polarity;~~

~~— said sample hold circuit includes a first comparing circuit comparing a charged voltage of said first charging charge circuit with a reference voltage;~~

a second comparing circuit comparing a charged voltage of said second charging charge circuit with a reference voltage;

a first sample hold circuit sampling and holding said charged voltage of said second charging charge circuit, based on a comparison result of said first comparing circuit; and

a second sample hold circuit sampling and holding said charged voltage of said first charging charge circuit, based on a comparison result of said second comparing circuit, and

wherein said outputting means outputs a first sampled and held voltage in said first sample hold circuit, according to said comparison result of said first comparing circuit, and outputs a second sampled and held voltage in said second sample hold circuit, according to said comparison result of said second comparing circuit.

**4. (Original)** The signal processing circuit as claimed in claim 3, wherein said first sample hold circuit includes a first switch circuit switched according to said comparison result of said first comparing circuit; and

a first capacitor charged according to said charged voltage of said second charge circuit, when said first switch circuit is switched on, and

said second sample hold circuit includes a second switch circuit switched according to said comparison result of said second comparing circuit; and

a second capacitor charged according to said charged voltage of said first charge circuit, when said second switch circuit is switched on.

**5. (Original)** The signal processing circuit as claimed in claim 3, wherein said first charge circuit includes a first constant current source outputting the constant current;

a first charging switch circuit switched on when said input pulse signal has a positive polarity so as to output said constant current output from said first constant current source;

a third capacitor charged with said constant current output from said first charging switch circuit, when said first charging switch circuit is switched on; and

a first discharging switch circuit switched on according to said comparison result of said second comparing circuit so as to discharge said third capacitor, and

said second charge circuit includes a second constant current source outputting the constant current;

a second charging switch circuit switched on when said input pulse signal has a negative polarity so as to output said constant current output from said second constant current source;

a fourth capacitor charged with said constant current output from said second charging switch circuit, when said second charging switch circuit is switched on; and

a second discharging switch circuit switched on according to said comparison result of said first comparing circuit so as to discharge said fourth capacitor.

**6. (Previously Amended)** The signal processing circuit as claimed in claim 4, wherein said first charge circuit includes a first constant current source outputting the first constant current;

a first charging switch circuit switched on when said input pulse signal has a positive polarity so as to output said first constant current output from said first constant current source;

a third capacitor charged with said constant current output from said first charging switch circuit, when said first charging switch circuit is switched on; and

a first discharging switch circuit switched on according to said comparison result of said second comparing circuit so as to discharge said third capacitor, and

said second charge circuit includes a second constant current source outputting the second constant current;

a second charging switch circuit switched on when said input pulse signal has a negative polarity so as to output said second constant current output from said second constant current source;

a fourth capacitor charged with said constant current output from said second charging switch circuit, when said second charging switch circuit is switched on; and

a second discharging switch circuit switched on according to said comparison result of said first comparing circuit so as to discharge said fourth capacitor.

**7. (Original)** The signal processing circuit as claimed in claim 2, wherein said charging circuit includes a constant current source generating a constant current;  
a first charge element charged with said constant current;  
a second charge element charged with said constant current; and  
a switch switched according to said input pulse signal so as to supply said first charge element with said constant current generated by said constant current source when said input pulse signal has the one of said polarities, and to supply said second charge element with said constant current generated by said constant current source when said input pulse signal has the other of said polarities.

**8. (Original)** The signal processing circuit as claimed in claim 2, wherein said outputting means comprises an output circuit outputting a voltage sampled and held in said sample hold circuit as the output signal.

**9. (Original)** The signal processing circuit as claimed in claim 3, wherein said outputting means comprises an output circuit outputting the voltage sampled and held in one of said first sample hold circuit and said second sample hold circuit, as the output signal.

**10. (Original)** The signal processing circuit as claimed in claim 4, wherein said outputting means comprises an output circuit outputting the voltage sampled and held in one of said first sample hold circuit and said second sample hold circuit, as the output signal.

**11. (Original)** The signal processing circuit as claimed in claim 5, wherein said outputting means comprises an output circuit outputting the voltage sampled and held in one of said first sample hold circuit and said second sample hold circuit, as the output signal.

**12. (Original)** The signal processing circuit as claimed in claim 6, wherein said outputting means comprises an output circuit outputting the voltage sampled and held in one of said first sample hold circuit and said second sample hold circuit, as the output signal.

**13. (Original)** The signal processing circuit as claimed in claim 7, wherein said outputting means comprises an output circuit outputting a voltage sampled and held in said sample hold circuit as the output signal.

**14. (Original)** The signal processing circuit as claimed in claim 9, wherein said output circuit includes a switch circuit selectively outputting either of said voltage sampled and held in said first sample hold circuit and said voltage sampled and held in said second sample hold circuit; and  
a switch control circuit switching said switch circuit so as to select said voltage sampled and held in said first sample hold circuit according to said comparison result of said first comparing circuit, and to select said voltage sampled and held in said second sample hold circuit according to said comparison result of said second comparing circuit.

**15. (Original)** The signal processing circuit as claimed in claim 10, wherein said output circuit includes a switch circuit selectively outputting either of said voltage sampled and held in said first sample hold circuit and said voltage sampled and held in said second sample hold circuit; and

a switch control circuit switching said switch circuit so as to select said voltage sampled and held in said first sample hold circuit according to said comparison result of said first comparing circuit, and to select said voltage sampled and held in said second sample hold circuit according to said comparison result of said second comparing circuit.

**16. (Original)** The signal processing circuit as claimed in claim 11, wherein said output circuit includes a switch circuit selectively outputting either of said voltage sampled and held in said first sample hold circuit and said voltage sampled and held in said second sample hold circuit; and  
a switch control circuit switching said switch circuit so as to select said voltage sampled and held in said first sample hold circuit according to said comparison result of said first comparing circuit, and to select said voltage sampled and held in said second sample hold circuit according to said comparison result of said second comparing circuit.

**17. (Original)** The signal processing circuit as claimed in claim 12, wherein said output circuit includes a switch circuit selectively outputting either of said voltage sampled and held in said first sample hold circuit and said voltage sampled and held in said second sample hold circuit; and  
a switch control circuit switching said switch circuit so as to select said voltage sampled and held in said first sample hold circuit according to said comparison result of said first comparing circuit, and to select said voltage sampled and held in said second sample hold circuit according to said comparison result of said second comparing circuit.

**18. (Currently Amended)** A signal processing method for outputting an output signal corresponding to a pulse width of an input pulse signal, the method comprising:



a step of gradually changing the charge in a first charging circuit when said input pulse signal is of positive polarity and gradually changing the charge in a second charging circuit when said input pulse signal is of negative polarity for a period of time to permit a noise component to be superimposed on at least one pulse;

\_\_\_\_\_ a step of sampling and holding the charge accumulated in each of the first and second charging circuits so as to generate said output signal;

\_\_\_\_\_ a step of accumulating the pulse widths of said input pulse signal for a predetermined period of time, each of the pulse widths having one of positive and negative polarities; and

a step of outputting the output signal corresponding to said accumulated pulse widths corresponding to the pulse width of each input pulse based on the charge accumulated in one of the first and second charging circuits.